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PATENT

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November 2, 2000
Date

Lisa Napoli
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Pierre C. Fazan and Gurtej S. Sandhu	Attorney Docket No.:	660073.488D1 (500055.02)
Serial No.	: 09/386,646	Group Art Unit	: 2811
Filed	: August 31, 1999	Examiner	: Hung K. Vu
Title	: METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION		

Commissioner for Patents
Washington, DC 20231

DECLARATION UNDER 37 C.F.R. § 1.131

Sir:

I, Gurtej S. Sandhu, hereby declare as follows:

1. I am a joint inventor, along with Pierre C. Fazan, of the invention described and claimed in U.S. Patent Application Serial No. 09/386,646, entitled METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION.

2. Prior to January 11, 1996, we, as joint inventors, had conceived and reduced to practice methods and apparatus featuring reduction or elimination of spacers about the edges of isolation pad structures on microelectronic devices as described in the subject patent application. On information and belief, all of the activities toward conception and reduction to practice described herein were conducted entirely within the United States, and more specifically, within the State of Idaho.

3. Attached hereto as Exhibit A is a true copy of confidential documentation created near the dates of conception and reduction to practice of the

disclosed embodiments. Exhibit A was prepared by myself and Mr. Fazan as the joint inventors named in this application. As shown on page 3 of Exhibit A, Mr. Fazan and I signed the document disclosing our invention on February 10, 1993, and the document was date-stamped received by the legal department of assignee Micron Technology, Inc. on February 10, 1993. In the copy attached hereto, some of the non-essential portions of Exhibit A have been redacted.

4. Figures 1 through 9 of Exhibit A correspond closely with Figures 1 through 2H of the subject patent application. Specifically, Figure 9 of Exhibit A (corresponding to Figure 1 of the patent application) shows a prior art microelectronic device having oxide spacers along the edges of a field oxide ("Fox") isolation pad. Figure 1 of Exhibit A (corresponding to Figure 2A of the patent application) shows a pad oxide or gate oxide layer formed on a surface of a microelectronic substrate. Figure 2 of Exhibit A (corresponding to Figure 2B of the patent application) shows a first gate layer ("poly gate") formed on the gate oxide layer, and a nitride stop layer ("nitride") formed on the first gate layer. Figure 3 of Exhibit A (corresponding to Figure 2C of the patent application) shows a trench formed through the nitride stop layer, first gate layer, gate oxide layer, and extending into the substrate. Figure 4 of Exhibit A (corresponding to Figure 2D of the patent application) shows the trench filled with field oxide to the level of the nitride stop layer after chemical-mechanical polishing (CMP). Figure 5 of Exhibit A (corresponding to Figure 2E of the patent application) shows the level of the field oxide within the trench lowered below the first gate layer, and the nitride stop layer removed. Figure 6 of Exhibit A (corresponding to Figure 2F of the patent application) shows a polysilicon adhesion layer ("Poly B") formed over the field oxide layer and the first gate layer ("Poly A"), and a conductive layer ("Wsix") formed on the polysilicon adhesion layer. Figure 7 of Exhibit A (corresponding to Figure 2G of the patent application) shows the patterning of the conductive layer, polysilicon adhesion layer, first gate layer, and gate oxide layer to form gate structures. Finally, Figure 8 of Exhibit A (corresponding to Figure 2H of the patent application) shows the formation of spacers adjacent the edges of the gate structures but not adjacent the edges of the field oxide isolation pad.

5. Furthermore, an embodiment of a method of forming trench isolation structures is described in detail on page 1 of Exhibit A. This embodiment

closely corresponds with the embodiment depicted in Figure 3 of the patent application.

6. It is my recollection that we diligently pursued and actually reduced to practice embodiments of the inventive methods and apparatus disclosed in the subject patent application, resulting in the fabrication of experimental or sample DRAM devices in accordance with the disclosed embodiments prior to January 11, 1996.

7. Specifically, we conceived and reduced to practice microelectronic devices according to the following claims of the subject patent application:

> 22. A microelectronic device, comprising:
>
> a microelectronic substrate;
>
> a structure including a gate oxide layer formed on the substrate and a first gate layer formed on the gate oxide layer, the structure having a trench at least partially disposed therein and extending into the substrate;
>
> a field oxide layer at least partially in the trench, the field oxide layer having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the first gate layer; and
>
> a polysilicon adhesion layer formed at least partially over the first gate layer and the field oxide layer.
>
> 26. A microelectronic device, comprising:
>
> a microelectronic substrate having a trench formed in a surface thereof;
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> a field oxide in the trench, the field oxide extending from the trench beyond the surface of the substrate; and
>
> a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.
>
> 28. A microelectronic device, comprising:
>
> a microelectronic substrate having a trench formed in a surface thereof;
>
> a field oxide in the trench, the field oxide extending from the trench beyond the surface of the substrate; and

a gate structure formed on the substrate, the gate structure extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

30. A microelectronic device, comprising:

a microelectronic substrate;

a gate oxide layer formed on the substrate and a first gate layer formed on the gate oxide layer, the first gate layer having a recess formed in a surface thereof and extending through the gate oxide layer and at least partially into the substrate;

a field oxide deposited in the recess, the field oxide extending from the recess beyond the surface of the substrate, by a height which is less than approximately one half of a height of the first gate layer formed on the field oxide and

a polysilicon adhesion layer formed at least partially over the first gate layer and the field oxide.

32. A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a gate structure formed on the substrate;

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate; and

an oxide spacer adjacent the gate structure.

34. A microelectronic device, comprising:

a microelectronic substrate;

a gate oxide layer formed on the substrate and a first gate layer formed on the gate oxide layer, the substrate having a trench formed therein at least proximate the first gate layer and the gate oxide layer;

a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide pad; and

a polysilicon adhesion layer formed at least partially over the first gate layer and the field oxide layer.

8. Also prior to January 11, 1996, we had conceived of alternate embodiments of such microelectronic devices. For example, we conceived of devices according to claim 22, wherein the first gate layer comprises a p lysilicon layer (claim 35), or wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the first gate layer/silicide layer (claim 36/claim 37), or further including a silicide layer formed over the polysilicon adhesion layer (claim 24), or further including a tungsten silicide layer formed over the polysilicon adhesion layer (claim 25). We also conceived of devices as recited in claims 26, 28, 30, and 32, further including an oxide spacer adjacent the component or gate structure, respectively (claims 27, 29, 31, and 33).

I certify and declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application

Signed this 9th day of November, 2000 at Boise, Idaho.

Gurtej S. Sandhu